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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,785	01/03/2002	Jeffrey B. Casady	2343-137-27	8552

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,785	CASADY ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 38-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 38-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 7-15 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Palmour (U.S. Pat. No. 5,270,554).

Regarding claim 1, Fig. 1 of Palmour shows a semiconductor device comprising

a substrate 10, a semi-insulating silicon carbide layer 12 on the substrate (col. 8, lines 38-44), and a semiconductor device (MESFET) formed on the semi-insulating silicon carbide layer, having an active area of a high band gap material 14(silicon carbide; col. 3, lines 22-25).

Regarding claim 2, Palmour shows the semi-insulating silicon carbide layer is formed epitaxially (col. 3, line 65).

In addition, note that "epitaxial growth" is a process designation and would not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 3, Palmour discloses the semi-insulating layer comprises boron (col. 8, lines 54-58).

Regarding claim 5, Palmour discloses the semiconductor device is a high frequency device (col. 1, line 12).

Regarding claim 7, Palmour discloses the substrate is a conductor (col. 3, lines 62-63).

Regarding claim 8, Palmour discloses the substrate is either n type or p type silicon carbide (col. 3, lines 62-63).

Regarding claims 9 and 10, Palmour discloses the semi-insulating silicon carbide layer Is 6H or 4H silicon carbide (col. 6, lines 3-4).

Regarding claim 11, Palmour discloses the semiconductor device comprises silicon carbide (col. 3, lines 22-25). Note that the semiconductor device is built on the SiC semi-insulating layer.

Regarding claims 12 and 13, Fig. 1 of Palmour shows the semiconductor device is a lateral MESTET. Palmour also discloses a MOSFET is used for high power applications (col. 1, lines 26-35).

Regarding claims 14 and 15, Palmour discloses a bipolar junction transistor and a JFET can be used for high power applications (col. 1, lines 26-35).

Regarding claims 19, Palmour discloses the first semiconductor device is formed epitaxially. In addition, note that "epitaxial growth" is a process designation and would not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 38-40 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Ajit (U.S. Pat. No. 6,310.385).

Regarding claim 38, Fig. 4 of Ajit shows a semiconductor device comprising

a conducting substrate (155 and 67), a semi-insulating silicon carbide layer 40 formed on the substrate (col. 3, lines 6-11), a first semiconductor device 20,10 over the substrate, a second device 10, 20 over the substrate and the semi-insulating silicon carbide layer insulating the first device from the second device.

Regarding claim 39, Fig. 4 of Ajit shows the first device formed over the first portion of the of the semi-insulating silicon carbide layer.

Regarding claims 40 and 44, Fig. 4 of Ajit shows a high power lateral device (col. 1, lines 11-14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmour in view of Barrett et al. (U.S. Pat. No.5,611,955).

Regarding claim 4, Palmour discloses substantially the entire claimed structure except for the semi-insulating layer comprising a transition metal. Barrett et al. teach that the semi-

insulating silicon carbide layer comprises transition metal (col. 2, lines 66-67 and col. 3, lines 27-66).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Barrett et al. to the device of Palmour in order to have a transition metal (vanadium) contained in SiC layer since vanadium in SiC would create deep level electronic states within the energy gap, thus causing high resistivity (semi-insulation behavior) in SiC as taught by Barrett et al. in col. 3, lines 57-66.

Regarding claim 6, Palmour discloses the semiconductor device is a high power device (Abstract, line).

Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Palmour in view of Fujita et al. (U.S. Pat. No. 4, 794, 608).

Regarding claims 16-18, Palmour does not explicitly disclose a second device(or multiple chips) built on an SiC semi-insulating layer on a SiC substrate. Fujita et al. show a multiple devices built on the substrate (col. 5, lines 59-63). It would have been obvious to one of ordinary skill in the art at the time of the invention to built a second chip (or multiple chip) on the same semi-insulating layer and the substrate of Palmour's device with the teaching of Fujita et al. in order to implement a circuit that requires more than one chip, as is usual in the art. And, it would have been obvious to have two chips electrically and physically isolated in order to have a chip operated individually.

Claims 41-43 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajit in view of Alok (U.S. Pat. No. 6,303,508)

Regarding claims 41, 43 and 45, Ajit shows substantially the entire claimed structure except the specific applications for the second device. Alok discloses high voltage devices include control circuitry on the same chip (col. 3, lines 38-43). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify one of Ajit's devices with the teaching of Alok to include a control device in order to reduce the power consumption in high voltage application and to form an integrated circuit including control circuit (col. 3, lines 41-47).

Regarding claim 42, Fig. 4 of Ajit shows substantially the entire claimed structure except the high frequency applications for the first device. Fig. 2 of Alok discloses two different devices built on SiC substrate, and discloses a high voltage and high frequency application (col. 1, lines 19-20). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Alok to the device of Ajit to have one of the device used for high frequency application to form a high frequency integrated circuit.

Regarding claim 46, Fig. 4 of Ajit shows substantially the entire claimed structure except the one of the devices being a vertical device. Fig. 2 of Alok show two device built on SiC substrate and one of the devices is a vertical device 140 (col.6, lines 2-3). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Alok to the device of Ajit to have a vertical device on order to fabricate a high power integrated circuit.

An additional reference of Kamiyama et al. (U.S. Pat. No.5,597,744) is introduced to show that a vertical device is built on an semi-insulating SiC layer on the SiC substrate. Fig. 8 show an substantially identical structure to pending invention.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMI
June 25, 2003

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800